Claims:

1. (original) A programmable audio processor chip for processing voice data comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data.

2. (original) The programmable audio processor chip of claim 1, wherein the chip is further adapted to convert the voice data between IP audio data and digital audio data.

3. (original) The programmable audio processor chip of claim 1, further comprising an analog-digital (A/D) converter adapted to convert the voice data between analog and digital form.

4. (original) The programmable audio processor chip of claim 3, wherein the A/D converter is adapted to convert voice data captured at a microphone of a telephony device employing the audio processor and to deliver the converted signal to the audio data converter.

5. (original) The programmable audio processor chip of claim 3, further comprising a telephony device that houses the audio processor, wherein the A/D converter is adapted to convert a digital signal received from the converter into analog form for use at a speaker of the telephony device.

6. (original) The programmable audio processor chip of claim 1, wherein IP network stack includes at least one of: a TCP/IP stack and a H.323 stack.

7. (original) The programmable audio processor chip of claim 1, wherein the communication stack is adapted to provide at least one of the following protocols: call setup, call tear down, capabilities exchange and negotiation.

8. (original) The programmable audio processor chip of claim 1, further comprising sufficient on-chip RAM to run a connection-less thin client call stack, a TCP/IP stack and audio compression protocols, wherein the processor is adapted to function without external system memory

9. (original) The programmable audio processor chip of claim 1, wherein the chip is adapted to dissipate 250 mW at 200 MHz.

10. (original) The programmable audio processor chip of claim 1, wherein the audio processing circuitry is programmed with a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity.

11. (original) The programmable audio processor chip of claim 1, wherein the audio processing circuitry is adapted to be programmed using C programming language.

12. (original) The programmable audio processor chip of claim 1, wherein the audio processing circuitry further comprises Flash-cache architecture adapted to enable a CPU to boot and run code from an external Flash-style device, and mix this execution space with memory on the chip.

13. (original) A telephony communications device adapted to communicate data including voice data, the device comprising:

a programmable audio processor chip having both microcontroller and DSP functions and adapted to perform Internet protocol/digital (IP/D) conversions for IP voice data and digital voice data;

an audio capture device communicatively linked to the programmable audio processor chip and adapted to capture voice data and communicate the captured voice data to the programmable audio processor chip; and

an audio speaker communicatively linked to the programmable audio processor chip and adapted to generate sound in response to data communicated from the programmable audio processor chip.

14. (original) The telephony communications device of claim 13, wherein the programmable audio chip comprises:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data.

15. (original) The telephony communications device of claim 13, wherein the device further comprises flash-style, non-volatile memory that includes embedded firmware for that device, and wherein the programmable audio processor chip includes a flash-cache architecture adapted to enable a CPU to boot and run code from an external Flash-style device and mix this execution space with memory at the chip.

16. (original) The telephony communications device of claim 15, further comprising a plurality of communications stacks, wherein the device is adapted to run compute-intensive DSP code out of internal RAM and to run the communication stacks out of external flash memory.

17. (original) The telephony communications device of claim 16, wherein the device is adapted to run DSP code including at least one of: audio codecs, acoustic echo cancellation and framing.

18. (original) The telephony communications device of claim 16, wherein the communication stacks are adapted to process data for executing at least one of: call setup, call teardown, capabilities exchange and negotiation.

19. (original) The telephony communications device of claim 13, wherein the chip includes a chip set having a plurality of chips, each of the plurality of chips being adapted to perform at least one selected function of the chip.

20. (original) An IP telephony communications network comprising:

a plurality of IP telephony devices each having a programmable audio processor chip comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data;

a CPU adapted to communicate with the plurality of IP telephony communications devices and to program the programmable audio processor chip in each IP telephony device, the programming including communications protocols, the CPU having a standard RISC 5-stage pipeline adapted to execute a plurality of instructions simultaneously; and

a communications link coupled to each of the IP telephony devices and to the CPU and adapted to transmit communications data including voice IP data.

21. (original) The network of claim 20, wherein the CPU further comprises a DSP Multiply Accumulate (DSPMAC) unit and an Address Generation Unit (AGU).

22. (original) The network of claim 21, wherein the AGU is adapted to effect address calculation concurrently with normal program flow address calculation of the CPU.

23. (original) The network of claim 22, wherein the DSPMAC and AGU are adapted to be used together in single instruction mnemonics.